REMARKS

Claims 1-4 are all the claims currently pending in this Application.

Information Disclosure Statement of February 6, 2006

Applicants note that with the current Office Action, the Examiner returned a copy of the PTO-SB-08 submitted with the Information Disclosure Statement of February 6, 2006, but that the Examiner had crossed out all the references listed thereon.

Applicants respectfully request an explanation of why these references were crossed out and respectfully request that a duly signed *and initialed* copy of this form be returned with the next Office communication, *without* the references crossed out.

Prior Art Rejections

Claims 1-4 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by Ikefuji (U.S. Patent 6,404,644). Applicants respectfully traverse this rejection.

Regarding claim 1, Applicants submit that Ikefuji fails to disclose or suggest "plural mounting pads connected to both ends of the circuit line formed on one surface of a base sheet, wherein the plural mounting pads are faced each other and spaced a pad clearance gap apart, and one of more semiconductor mounting paste guide paths are formed in the mounting pads," as recited in claim 1. Regarding the mounting pads, the Examiner asserts that Ikefuji "discloses a flip chip mounting substrate which comprises: an electronic circuit composed of a circuit line (element 12, Figs 1-4, 32, Fig 5,52, 57, Figure 6) and plural mounting pads (element 12a, 12b, Figs 1-4_ connected to both ends of the circuit line formed on one surface of a base sheet (element 10, Figs 1-4)." However, element 21a of Ikefuji is a coil outer end, and element 12b is a

coil inner end. Neither these elements, nor any other portion of Ikefuji teaches or describes mounting pads.

Further, element 12a which is a coil outer end, and element 12b which is a coil inner end do not face each other and are not spaces a pad clearance gap apart, as recited.

Further, the Examiner asserts that Ikefuji "discloses wherein a broad section (element 19b, Figs 1-4) for pressing out and spreading uniformly the semiconductor mounting paste (element 19, Figs 1-4) to connecting to an IC chip is formed in a part of the pad clearance gap" and that Ikefuji discloses "therein a thin film layer (element 19a, Figs 1-4) is formed in center section of the broad section."

However, element 19 of Ikefuji is anisotropic conducting adhesive film and does not teach or describe semiconductor mounting paste. Ikefuji element 19a is a conductive portion to connect the coil inner end 12b and the terminal 11b of the IC chip 11. The element 19a does not teach or describe thin film layer which is formed in a center section of a broad section.

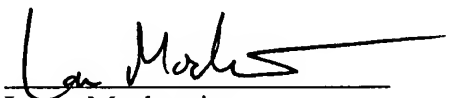
Therefore in view of the above, Applicants submit that claim 1 is patentable over the cited reference and that claims 2-4 are patentable at least by virtue of their dependence on claim 1. Applicants respectfully request that the rejection of claims 1-4 be reconsidered and withdrawn.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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